AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions:

1. (Currently Amended) A processor comprising:

a first functional unit to execute a first stream of instructions;

a second functional unit to execute a second stream of instructions;

a first local voltage regulator to provide a first local supply voltage to the first functional unit, said first local voltage regulator to reduce the first local supply voltage based at least in part on a particular time period between instructions in the first stream of instructions;

a second local voltage regulator to provide a second local supply voltage to the second functional unit, said second local voltage regulator to reduce the second local supply voltage based at least in part on a particular time period between instructions in the second stream of instructions; and

~~a plurality of circuit blocks;~~

~~a plurality of local voltage regulators to each independently provide a local supply voltage to one of the plurality of circuit blocks, each of the plurality of local voltage regulators being co-located with the circuit block powered by the respective local supply voltage; and~~

a global power grid to power ~~each of the plurality of~~ the first and second local voltage regulators with a global supply voltage.

2. (Currently Amended) The processor of claim 1, wherein at least one of the first and second local supply voltages is adjustable by the processor.

3. (Currently Amended) The processor of claim 2, wherein at least one of the first and second ~~plurality of~~ voltage regulators includes a digitized resistor to be set by the processor.

4. (Currently Amended) The processor of claim 1, wherein at least one of the first and second local supply voltages is to be set to allow the respective ~~circuit block~~ functional unit to meet a timing requirement.

5. (Previously Presented) The processor of claim 1, further comprising a port to receive the global supply voltage from an external voltage regulator.

6. (Currently Amended) The processor of claim 1, wherein at least one of the ~~plurality of~~ first and second local voltage regulators includes an op amp.

7. (Currently Amended) The processor of claim 1, wherein the first functional unit is selected from a group comprising a branch prediction unit, a floating point unit, and an integer unit ~~at least one of the plurality of circuit blocks comprises a digital circuit~~.

Claims 8-10. (Cancelled)

11. (Currently Amended) A computer system comprising:

a discrete voltage regulator to provide a global supply voltage; and

a processor including

a first functional unit to execute a first stream of instructions;

a second functional unit to execute a second stream of instructions;

a first local voltage regulator to provide a first local supply voltage to the first functional unit, said first local voltage regulator to reduce the first local supply voltage based at least in part on a particular time period between instructions in the first stream of instructions;

a second local voltage regulator to independently provide a second local supply voltage to the second functional unit, said second local voltage regulator to reduce the second local supply voltage based at least in part on a particular time period between instructions in the second stream of instructions; and

~~a plurality of circuit blocks,~~

~~a plurality of local voltage regulators to each independently provide a local supply voltage to one of the plurality of circuit blocks, each of the plurality of local voltage regulators being co-located with the circuit block powered by the respective local supply voltage, and~~

a global power grid to power ~~each of the plurality of~~ the first and second local voltage regulators with the global supply voltage.

12. (Currently Amended) The computer system of claim 11, wherein at least one of the first and second local supply voltages is adjustable by the processor.

13. (Currently Amended) The computer system of claim 12, wherein at least one of the ~~plurality of~~ first and second local voltage regulators includes a digitized resistor to be set by the processor.

14. (Cancelled)

15. (Original) The computer system of claim 11, wherein the processor is a graphics controller.

16. (Currently Amended) A method comprising:

providing a global supply voltage to a first local voltage regulator and a second local voltage regulator in a processor;

providing a first local supply voltage from the first local voltage regulator to a first functional unit to execute a first stream of instructions;

reducing the first local supply voltage based at least in part on a particular time period between instructions in the first stream of instructions;

providing a second local supply voltage from the second local voltage regulator to a second functional unit to execute a second stream of instructions; and

reducing the second local supply voltage based at least in part on a particular time period between instructions in the second stream of instructions;

~~providing a global supply voltage to a plurality of local voltage regulators through a global power grid, each of the plurality of local voltage regulators being co-located with one of a plurality of circuit blocks within a processor; and~~

~~independently providing a local supply voltage from each of the plurality of local voltage regulators to power a respective one of the plurality of circuit blocks.~~

17. (Currently Amended) The method of claim 16, wherein ~~independently~~ providing the first local supply ~~voltages~~ voltage comprises:

adjusting ~~at least one of~~ the first local supply ~~voltages~~ voltage by the processor.

18. (Currently Amended) The method of claim 16, wherein ~~one of the circuit blocks~~ the first functional unit comprises a floating point unit of the processor, and wherein ~~independently~~ providing the first local supply ~~voltages~~ voltage comprises powering the floating point unit.